REMARKS/ARGUMENTS

This application has been reviewed in light of the final Office Action mailed on September 15, 2009. Claims 1, 2, 4-9, 11-13, 15, 16, 18-20 and 22-27 are pending in the application with Claims 1, 8, 15, and 22 being in independent form. By the present amendment, Claims 1, 8 and 15 have been amended. Support for the amendments can be found throughout Applicants' specification. No new matter or issues are believed to be introduced by the amendments. Support for the new and amended claims can be found throughout the specification and drawings, and for example, in paragraphs [0039], [0040], [0046], and [0055] – [0060]; Tables 3, 6 & 7; and FIGs. 4B & 7.

I. Rejection Under 35 U.S.C. Section 132(a)

The specification is objected to under 35 U.S.C. Section 132(a). Claims 1, 8, 15, and 22 have been amended in a manner which is believed to expedite the prosecution of the present application. Accordingly, withdrawal of the objection is respectfully requested.

II. Rejection Under 35 U.S.C. Section 112

Claims 1-2, 4-9, 11-13, 15-16, and 18-20 are rejected under 35 U.S.C. Section 112, first paragraph. Independent Claims 1, 8, 15, and 22 have been amended in a manner which is believed to expedite the prosecution of the present application. Accordingly, withdrawal of the rejection is respectfully requested.

III. Rejection Under 35 U.S.C. Section 103

Claims 1, 4-5, 7-8, 11-12, 14 (previously cancelled), 15, and 18-19 are rejected under 35 U.S.C. Section 103 over Strolle et al. U.S. Patent Application Publication 2004/0028076 ("Strolle") in view of Birru et al. U.S. Patent Application Publication 2003/0099303 ("Birru") in view of Limberg U.S. Patent Application Publication 2004/0237024 ("Limberg I"); Claims 2, 9, and 16 are rejected under 35 U.S.C. Section 103 over Strolle in view of Birru in view of Limberg I as applied to Claims 1, 8, and 15 above, and further in view of Hurst, Jr. U.S.

Patent 6,034,731 ("Hurst"); Claims 6, 13, and 20 are rejected under 35 U.S.C. Section 103 over Strolle in view of Birru in view of Limberg I as applied to Claims 5, 12, and 19 above, and further in view of Fimoff U.S. Patent Application Publication 2001/0055342 ("Fimoff"); and Claims 22, 26, and 27 are rejected under 35 U.S.C. Section 103 over Strolle in view of Limberg U.S. Patent 6,621,527 ("Limberg II").

Applicants respectfully submit that all of the claims are patentable over the cited art for at least the following reasons.

Claim 1

Among other things, the packet formatter of Claim 1 includes a second processing block capable of determining the locations of the parity bytes within each robust packet according to the robust packet's position within the frame, in response to which the first processing block removes the header bytes and parity bytes from the dual bitstream signal to output a first output signal.

Applicants respectfully submit that no combination of the cited references would ever produce a packet formatter including this combination of features.

Strolle discloses a bitstream that includes normal packets and robust packets. Strolle also discloses that when a standard Reed-Solomon encoder is employed to generate the normal packets, then the parity bytes are output at the end of the decoded normal packets generated by a corresponding Reed-Solomon encoder. Strolle also discloses that when a non-standard Reed-Solomon encoder is employed to generate the robust packets, then the parity bytes in the robust packets are relocated so that the parity bytes all come out of the corresponding non-standard Reed-Solomon decoder first for the decoded robust packets. See paragraphs [0061]-[0063].

Strolle also discloses that the locations of the robust packets and the normal packets within a frame are known by reference to a robust mode tier control code value which is communicated to the receiver. See paragraph [0049].

Strolle further discloses that, at the receiver, the non-standard Reed-Solomon decoder must reorder the bytes for each packet depending on whether it is a robust packet or a normal packet, which can be determined from where the packet is located in the frame (using the

robust mode tier control code value). See paragraphs [0083]-[0084].

It is evident from the above description that in <u>Strolle</u> the locations of the parity bytes in the robust packets are different than the locations of the parity bytes in the normal packets. However, the locations of the parity bytes in all of the robust packets are the same as each other so that the parity bytes for each robust packet always come out of the non-standard Reed-Solomon decoder first.

Therefore, Applicants respectfully submit, and as acknowledged by the Examiner in the final Office Action, Strolle does not disclose a second processor block capable of determining the locations of the parity bytes of a robust packet according to the robust packet's position within the frame. Indeed, as explained above, Applicants respectfully submit that Strolle teaches that the locations of the parity bytes within each robust packet are the same as each other regardless of the robust packet's position within the frame.

Also among other things, the packet formatter of Claim 1 includes a third processing block capable of receiving a first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter.

The final Office Action fairly admits that <u>Strolle</u> does not disclose the recited third processing block. However, the final Office Action alleges that <u>Limberg I</u> discloses a third processing block including these features, and proposes to modify a combined <u>Strolle-Birru</u> system to include the third processing block of Claim 1.

Applicants traverse the proposed combination of <u>Strolle</u>, <u>Birru</u>, and <u>Limberg I</u> for at least the following reasons.

At the outset, Applicants respectfully submit that the final Office Action fails to establish the level of ordinary skill in the art of invention of Claim 1. This is a fundamental requirement for maintaining a rejection under 35 U.S.C. § 103. See M.P.E.P. §§ 2141(II)(C) and 2141.03. Thus, the final Office Action fails to perform the analysis required by KSR International Co. v. Teleflex Inc., 550 U.S. 398, 82 USPQ2d 1385 (2007) ("KSR") for rejecting a claim under 35 U.S.C. § 103.

Furthermore, a rejection on obviousness grounds under 35 U.S.C. § 103 cannot be sustained by mere conclusory statements: instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. See M.P.E.P. § 2142 (quoting In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) and KSR 82 USPQ2d at 1396 (2007) (quoting Federal Circuit statement with approval)).

Applicants respectfully submit that the proposed combination of <u>Strolle</u>, <u>Birru</u>, and <u>Limberg I</u> to attempt to construct the method of Claim 1 is not based on an articulated reasoning with any rational underpinnings, but instead is based on conclusory statements which lack reason.

The final Office Action states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method of <u>Limberg1</u> into a system formed by a combination of <u>Strolle</u> and <u>Birru</u> to add a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter, "in order to remove error correction bits (redundant bits) performed (sic) by the Forward Error Correction Coders."

However, Applicants respectfully submit that <u>Strolle</u>'s transmit system and <u>Birru</u>'s digital signal transmission system do not transmit a signal where each packet includes such duplicate bits ("redundant bits"). So modifying <u>Strolle</u> and/or <u>Birru</u> to add a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter, would not "remove error correction bits (redundant bits)" – because <u>no such bits exist</u> in the systems of <u>Strolle</u> and <u>Birru</u> to be removed. Indeed, all that the proposed modification would do is to turn <u>Strolle</u>'s receiver and/or <u>Birru</u>'s transmission system into a non-functional device and system, respectively, that would output incorrect data. Thus, Applicants respectfully submit that there is no reason for the proposed combination, and that the proposed combination is improper.

Therefore, for at least these reasons, Applicants respectfully submit that Claim 1 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of

Claim 1 be withdrawn and that Claim 1 be allowed.

Claim 8

Among other things, the method of Claim 8 includes: determining the locations of the parity bytes within a robust packet according to the robust packet's position within its frame; and removing from a first output signal duplicate bits associated with a robust stream to thereby produce a second output signal that is output from a data path output of a packet formatter.

As explained above with respect to Claim 1, Applicants respectfully submit that the prior art does not teach any method including such a combination of features. Applicants also respectfully traverse the proposed combination of <u>Strolle</u>, <u>Birru</u>, and <u>Limberg I</u> for at least the reasons set forth above with respect to Claim 1.

Therefore, for at least these reasons, Applicants respectfully submit that Claim 8 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of claim 8 be withdrawn and that Claim 8 be allowed.

Claim 15

Among other things, the receiver of Claim 15 includes: (1) a second processing block capable of determining the locations of the parity bytes within the current packet according to the current packet's position within its frame, in response to which a first processing block removes the header bytes and parity bytes from dual bitstream signal to output a first output signal; and (2) a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with a robust stream to thereby produce a second output signal that is output from a data path output of a packet formatter.

As explained above with respect to Claim 1, Applicants respectfully submit that the prior art does not teach any method including such a combination of features. Applicants also respectfully traverse the proposed combination of proposed combination of <u>Strolle</u>, <u>Birru</u>, and <u>Limberg I</u> for at least the reasons set forth above with respect to Claim 1.

Therefore, for at least these reasons, Applicants respectfully submit that Claim 15 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of Claim 15 be withdrawn and that Claim 15 be allowed.

Claims 2, 4-7, 9, 11-13, 16, and 18-20

Claims 2, 4-7, 9, 11-13, 16, 18-20 depend respectively from Claims 1, 8, and 15, and are deemed patentable over the cited art for at least the reasons set forth above with respect to claims 1, 8, and 15, and for the following additional reasons.

Claims 2, 9, and 16

Claims 2, 9, and 16 depend respectively from Claims 1, 8 and 15. Applicants respectfully submit that <u>Hurst</u> does not remedy the defects of <u>Strolle</u>, <u>Birru</u> and <u>Limberg I</u> as set forth above with respect to Claims 1, 8, and 15. Therefore, Claims 2, 9, and 16 are deemed patentable over the cited art for at least the reasons set forth above with respect to Claims 1, 8, and 15, and for the following additional reasons.

Claims 2, 9, and 16 all include a feature of passing bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time.

The Office Action states that <u>Hurst</u> teaches this feature.

Applicants respectfully disagree.

<u>Hurst</u> teaches that an MPEG picture header contains a delay number that indicates that indicates the mount of time that a video decoder should wait after the picture header enters the decoder's video buffer before decoding the picture.

<u>Hurst</u> does not teach passing bytes associated with the standard stream to the data path output of a packet formatter after delaying the standard stream bytes by a predetermined delay time. So no combination of <u>Hurst</u> with <u>Strolle</u>, <u>Birru</u> and <u>Limberg I</u> teaches the subject matter of Claims 2, 9, and 16.

Applicants also respectfully traverse the proposed combination of <u>Hurst</u> with <u>Strolle</u>, <u>Birru</u> and <u>Limberg I</u> as lacking any reason to combine.

Applicants respectfully submit that the proposed combination would not synchronize audio and video packets. The elements in <u>Strolle</u> cited in the final Office Action as supposedly corresponding to the recited packet formatter are all operating on <u>transmission</u> packets, which will of course include both audio packets and video packets – as well as other packets. Therefore any delay applied to packets by such as packet formatter would be also

applied to both audio packets and video packets, and would not perform any the "synchronization" which is proposed as the reason for the modification of Strolle.¹

Accordingly, for at least this additional reason, Applicants respectfully submit that Claims 2, 9, and 16 are patentable over the cited art.

Claims 6, 13, and 20

Claims 6, 13, and 20 depend respectively from Claims 1, 8, and 15. Applicants respectfully submit that <u>Fimoff</u> does not remedy the defects of <u>Strolle</u>, <u>Birru</u> and <u>Limberg I</u> as set forth above with respect to Claims 1, 8, and 15. Therefore, Claims 6, 13, and 20 are deemed patentable over the cited art for at least the reasons set forth above with respect to Claims 1, 8, and 15.

Claims 22, 26, and 27

Among other things, the data re-randomizer of Claim 22 includes a robust derandomizer and a delay calculation circuit for applying a control signal to the robust derandomizer to cause the robust de-randomizer to suspend its operation for a portion of a field in accordance with a determined delay. Applicants respectfully submit that the cited art does not disclose or suggest a data re-randomizer that includes this feature. Therefore, for at least these reasons, Applicants respectfully submit that Claim 22 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of Claim 22 be withdrawn and that Claim 22 and its dependent Claims 26 and 27 be allowed.

CONCLUSION

In view of the foregoing amendments and remarks, it is respectfully submitted that all Claims presently pending in the application, namely, Claims 1, 2, 4-9, 11-13, 15, 16, 18-20, and 22-27, are believed to be in condition for allowance.

¹ Also note, for example, that in Claim 19 the second processing block is clearly recited as preceding even the Reed Solomon decoder. Thus the second processing block which delays the standard stream bytes by a predetermined delay time, operates on packets before they are ever decoded and demultiplexed into video and audio packets, and before video packets could be reassembled into video frames and presented to a video decoder.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to contact the undersigned.

Respectfully submitted,

Kevin C. Ecker, Esq.

Registration No. 43,600

Date: November 9, 2009

By: George Likourezos

Reg. No. 40,067

Attorney for Applicants

631-501-5706

Mail all correspondence to: Kevin C. Ecker, Esq. Senior IP Counsel Philips Electronics North America Corp. P.O. Box 3001 Briarcliff Manor, New York 10510-8001

Phone: (914) 333-9618